CLAIMS

We claim:

1. An apparatus for testing a memory cell, the memory cell comprising a select transistor and a data storage element, said select transistor having a gate connected to a select wordline, a source connected to a first terminal of said data storage element, and a drain connected to a column bitline, said apparatus comprising:

a first column transistor connected to said column bitline;

a wordline decoder connected to said gate of said select transistor through said select wordline, said wordline decoder providing an output signal to said select transistor to activate said select transistor, said wordline decoder also providing a test voltage to be applied to a second terminal of said data storage element;

a sense amplifier that compares an input voltage to a reference voltage, said sense amplifier indicating that said memory cell tests programmable if said input voltage is higher than said reference voltage, said input voltage indicative of a Fowler-Nordheim current flowing through said data storage element.

2. The apparatus of Claim 1 wherein said test voltage is less than a programming voltage of said data storage element.

3. The apparatus of Claim 1 wherein the data storage element is a MOS capacitor.

4. The apparatus of Claim 1 wherein said data storage element comprises a conductive structure forming said second terminal, an ultra-thin dielectric underlying said conductive for physical storage of data, and a doped semiconductor region forming said first terminal underlying both the ultra-thin dielectric and the conductive structure.

5. The apparatus of Claim 1 further including a second column transistor in series with said first column transistor and on said bitline, wherein said input voltage is taken from between said first and second column transistor.

6. The apparatus of Claim 1 further including a control circuit that receives an output from said sense amplifier indicative of the programmability of said data storage element, said control circuit operative to terminate said test voltage if said data storage element tests programmable.

7. An apparatus for testing a memory cell, the memory cell comprising a select transistor and a data storage element, said select transistor having a gate connected to a select wordline, a source connected to a first terminal of said data storage element, and a drain connected to a column bitline, said apparatus comprising:

a first column transistor connected to said column bitline;

a wordline decoder connected to said gate of said select transistor through said select wordline, said wordline decoder capable of turning on said select transistor, said wordline decoder also capable of providing a test voltage to a second terminal of said data storage element;

means for measuring a current flowing through said data storage element when said test voltage is applied and providing a tests programmable signal if said current flow is greater than a reference.

8. The apparatus of Claim 7 wherein said test voltage is less than a programming voltage of said data storage element.

9. The apparatus of Claim 7 wherein the data storage element is a MOS capacitor.

10. The apparatus of Claim 7 wherein said data storage element comprises a conductive structure forming said second terminal, an ultra-thin dielectric underlying said conductive for physical storage of data, and a doped semiconductor region forming said first terminal underlying both the ultra-thin dielectric and the conductive structure.

11. The apparatus of Claim 7 further including a second column transistor in series with said first column transistor and on said bitline, wherein said input voltage is taken from between said first and second column transistor.

12. The apparatus of Claim 7 further including a control circuit that receives an output from said means for measuring current indicative of the programmability of said data storage element, said control circuit operative to terminate the test voltage if said data storage element tests programmable.

13. The apparatus of Claim 7 wherein said current is a Fowler-Nordheim current.

14. The apparatus of Claim 7 wherein said wordline decoder terminates said test voltage after a predetermined amount of time regardless of the amount of said current.

15. A method of testing the programmability of a memory cell, the memory cell comprising a select transistor and a data storage element, said select transistor having a gate connected to a select wordline, a source connected to a first terminal of said data storage element, and a drain connected to a column bitline, said method comprising:

applying a test voltage across said data storage element;

turning on said select transistor; and

measuring a current flow through said data storage element when said test voltage is applied and providing a test positive signal if said current flow is greater than a reference.

16. The method of Claim 15 wherein said reference is a reference current.

17. The method of Claim 15 wherein said current flow is converted to a voltage and said reference is a reference voltage.

18. The method of Claim 15 wherein said current flow is a Fowler-Nordheim current.

19. The method of Claim 15 wherein said test voltage is less than a programming voltage of said data storage element.

20. The method of claim 19 wherein said test voltage is applied for a time period substantially the same as or less than the time needed to read said data storage element.

21. The method of claim 19 wherein said test voltage is applied for a time period substantially less than the time needed to program said data storage element.

22. A method of programming a byte of a memory array with input data by applying a program pulse, the method comprising:

initially programming said byte into said memory array on a bit by bit basis using said program pulse;

verifying each bit in the byte as being programmed;

if the bit verifies correctly as programmed, changing the input data for said verified bit to a "0"; and

if the bit does not verify correctly, leaving the input data for said bit as-is, thereby allowing another program pulse to be applied to the unverified bit.

23. The method of Claim 22 wherein said verify step is performed at a reduced voltage than the program pulse.

24. The method of Claim 22, wherein said verify step is a reference level of a sensed current is altered to provide a necessary margin.